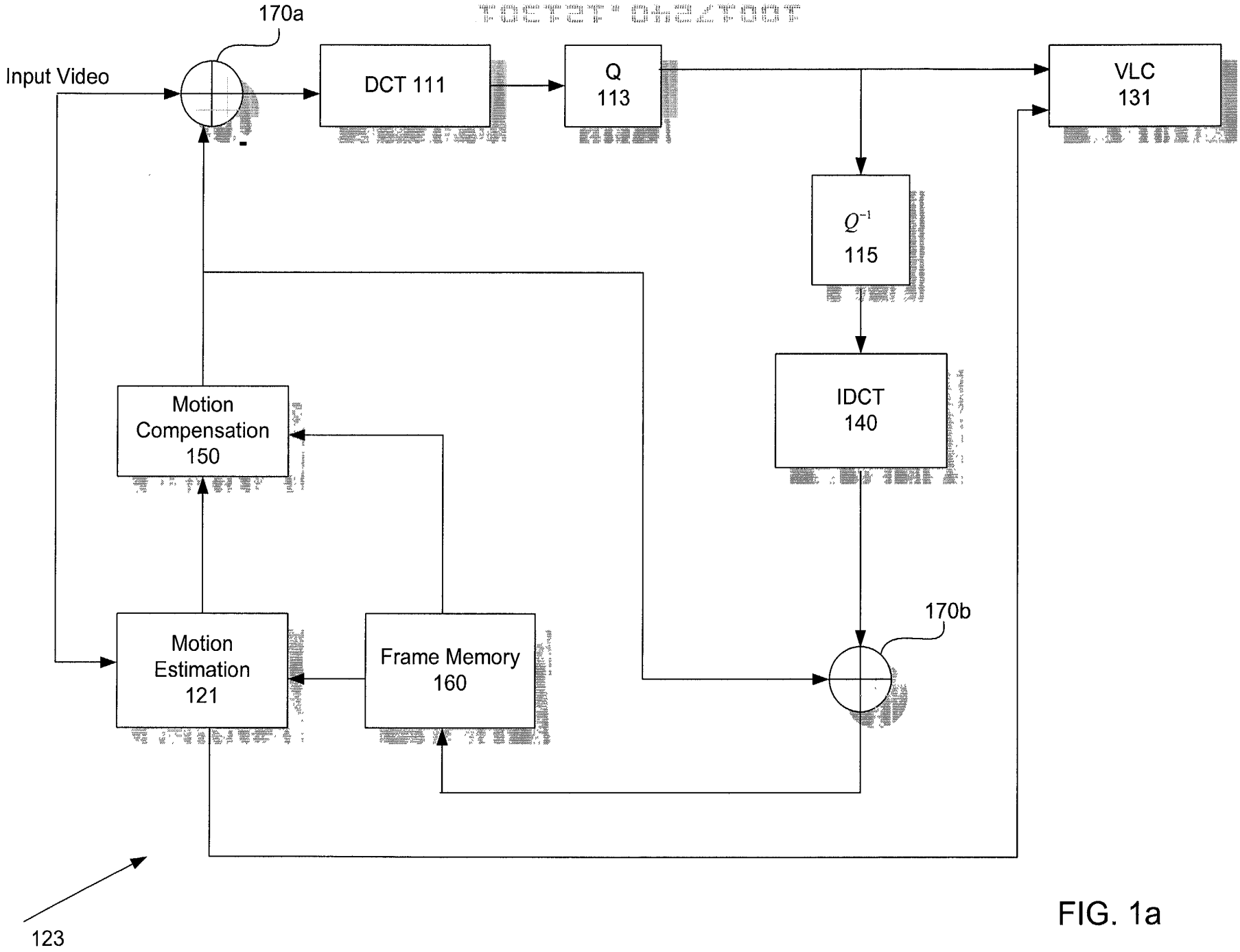

170a
Input Video
DCT 111
Q
113
VLC
131
Q^{-1}
115
IDCT
140
Motion
Compensation
150
Motion
Estimation
121
Frame Memory
160
170b
123

FIG. 1a

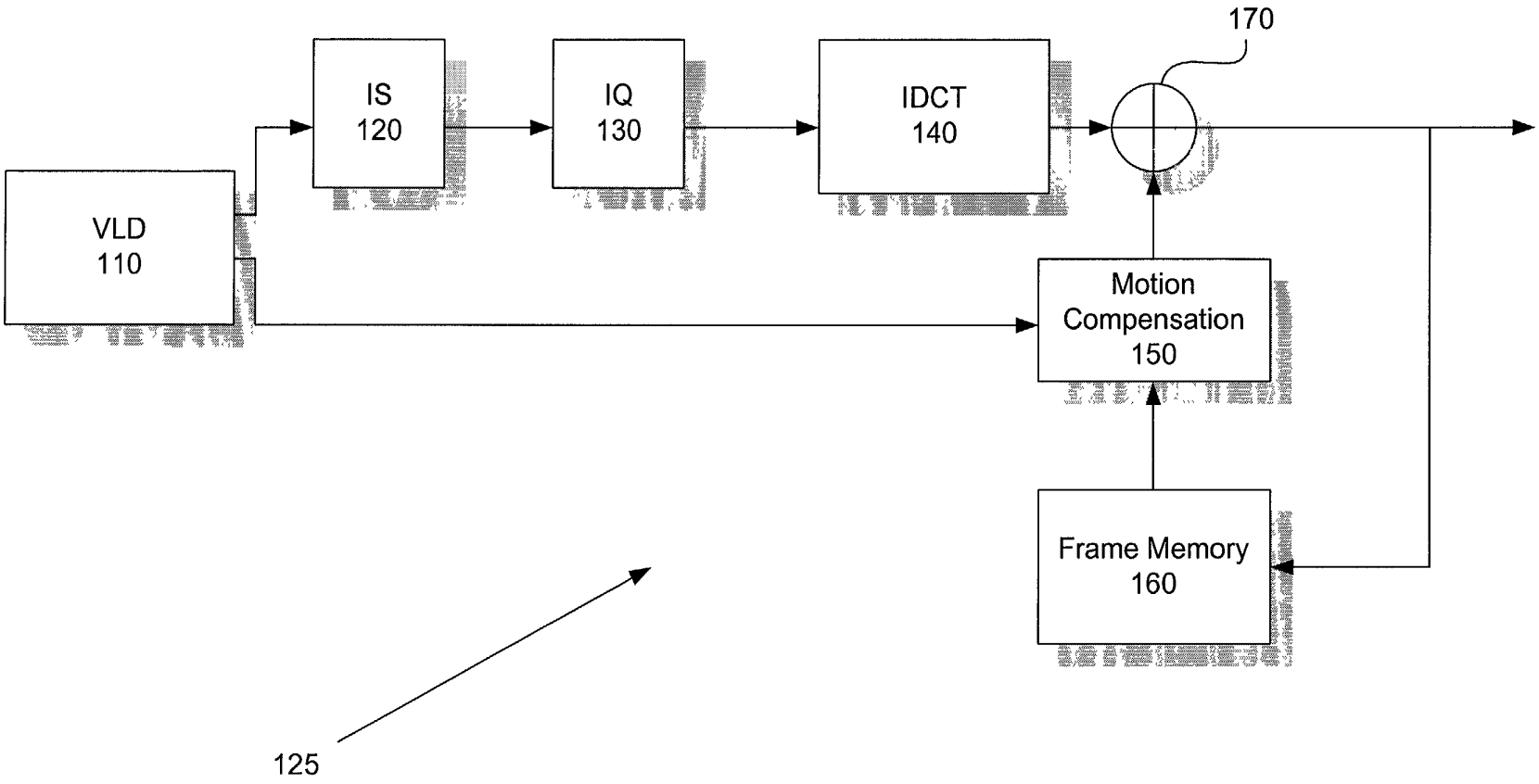

170
IS
120
IQ
130
IDCT
140
VLD
110
Motion
Compensation
150
Frame Memory
160
125

FIG. 1b

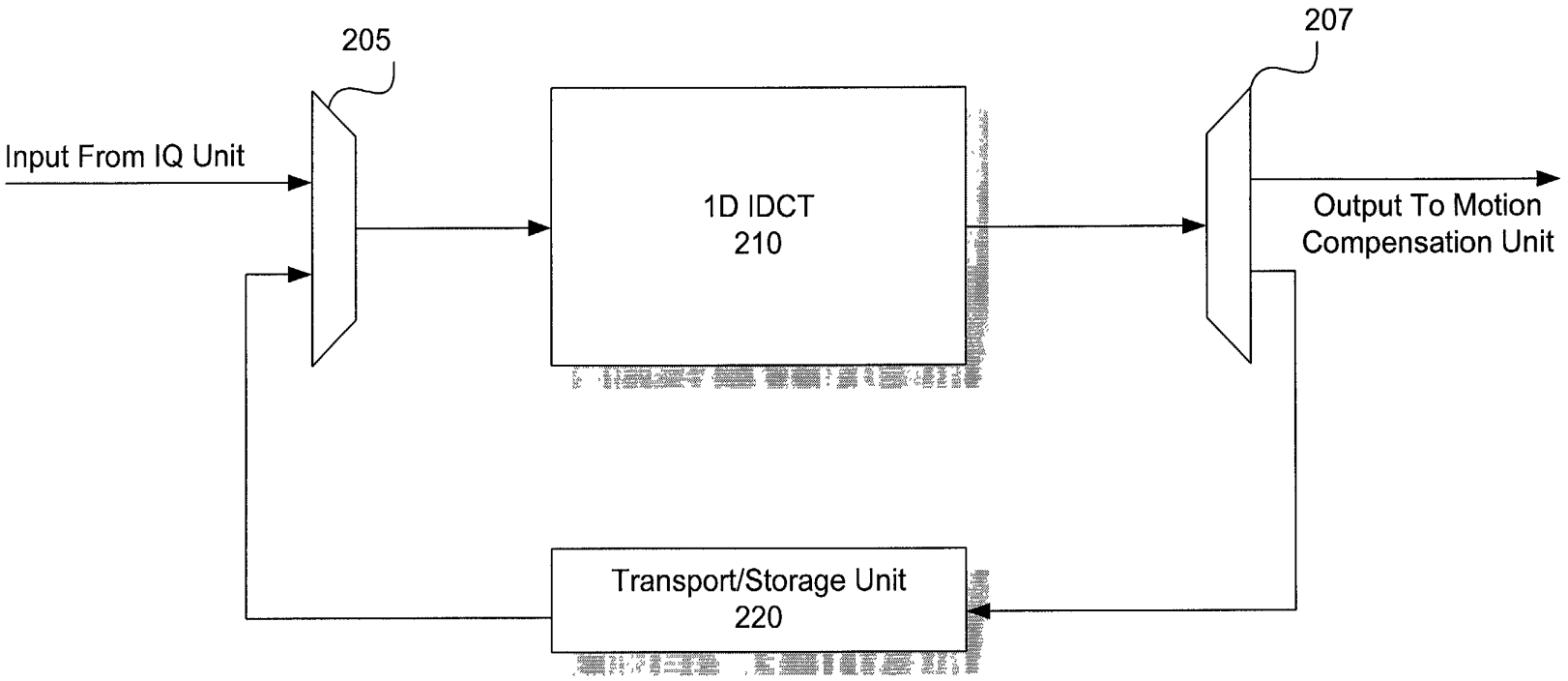


FIG. 2

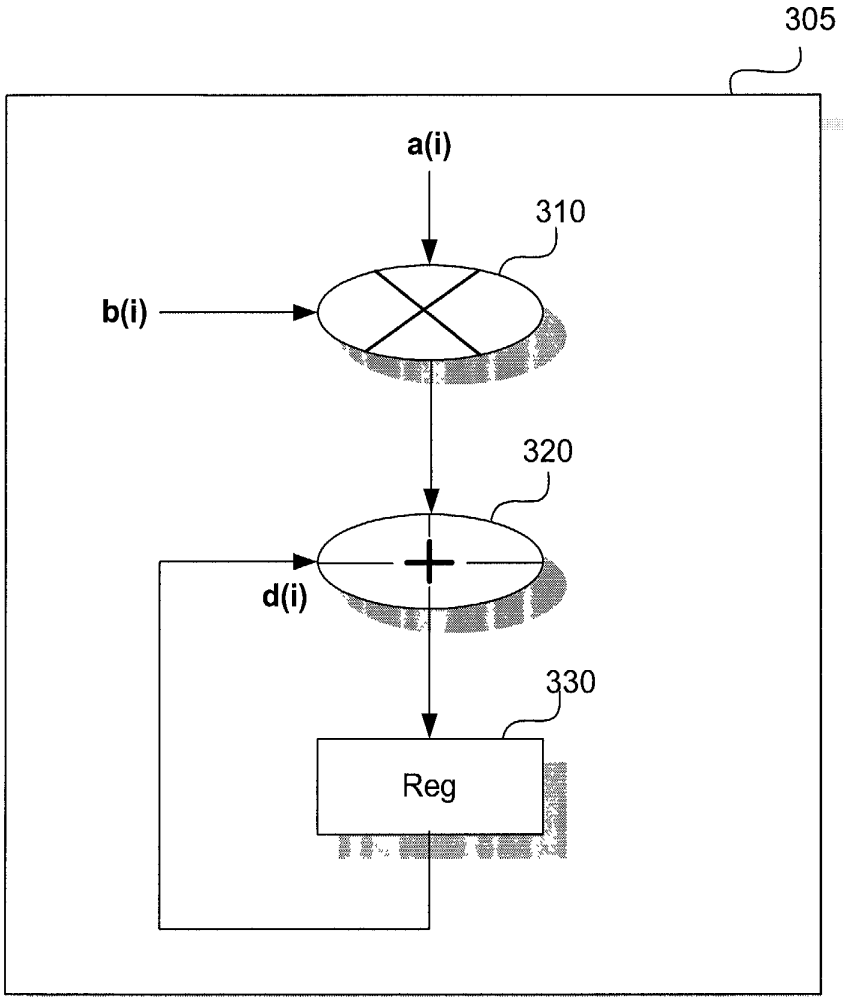


FIG. 3

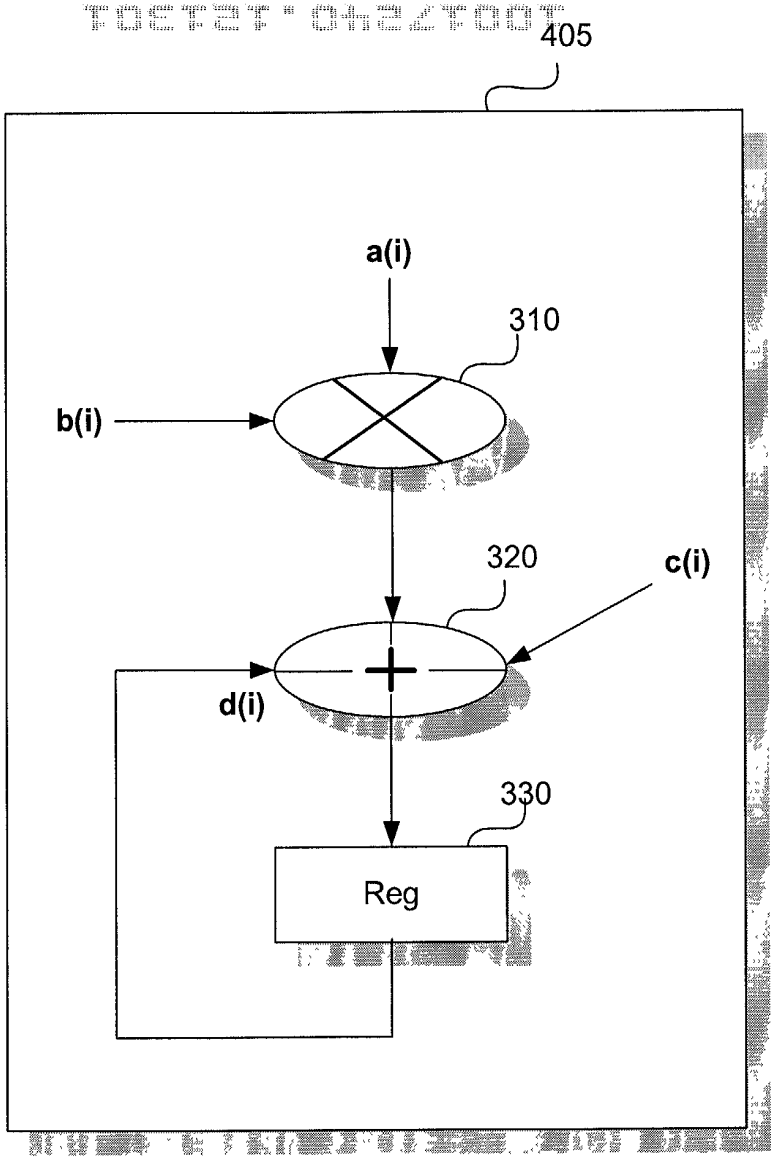


FIG. 4

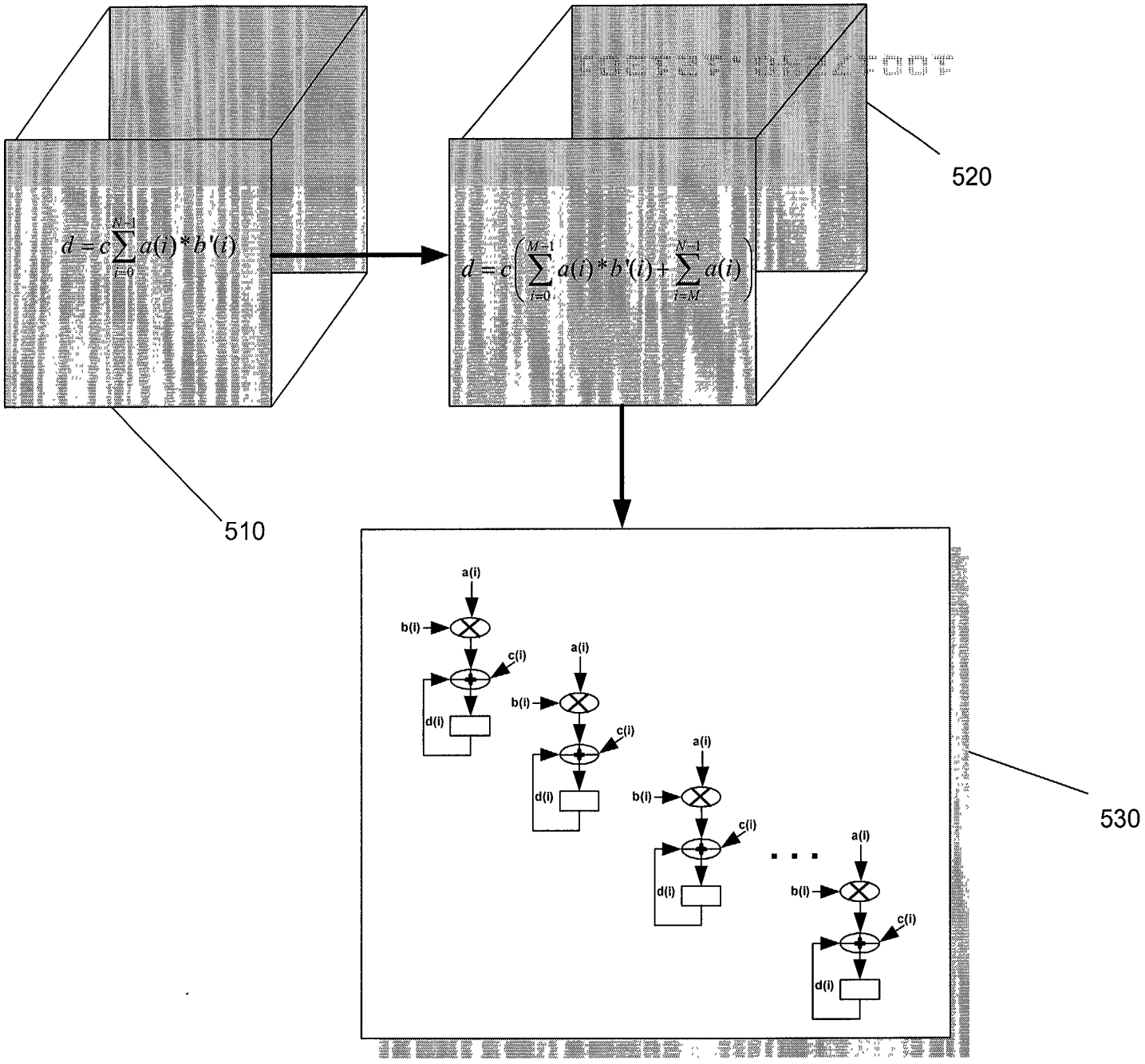

$d = c\sum_{i=0}^{N-1} a(i) * b'(i)$
$d = c\left(\sum_{i=0}^{M-1} a(i) * b'(i) + \sum_{i=M}^{N-1} a(i)\right)$
510
520
530
a(i)
b(i)
c(i)
d(i)

FIG. 5

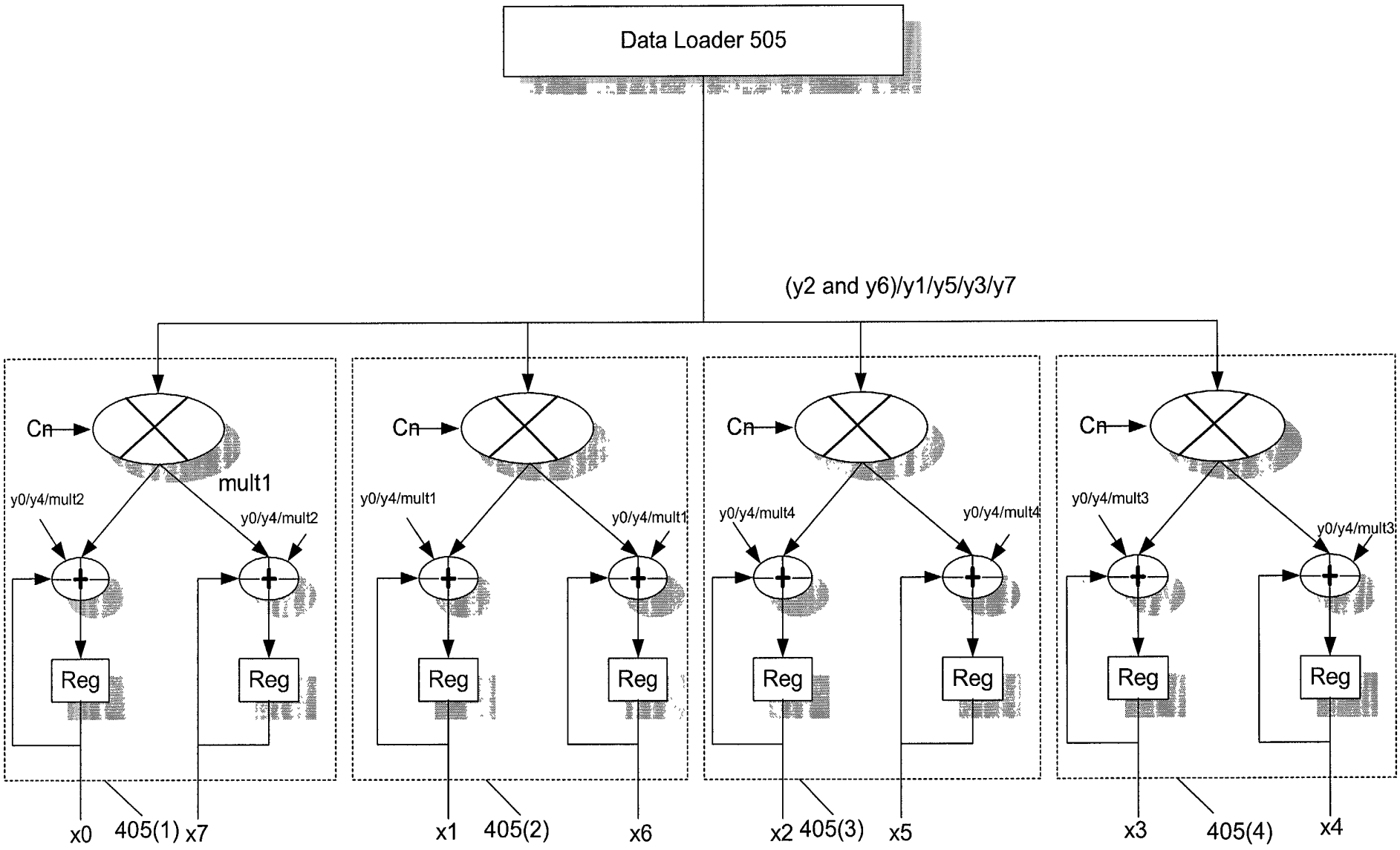

Data Loader 505
(y2 and y6)/y1/y5/y3/y7
Cn
mult1
y0/y4/mult2
y0/y4/mult2
Reg
Reg
x0
405(1)
x7
Cn
y0/y4/mult1
y0/y4/mult1
Reg
Reg
x1
405(2)
x6
Cn
y0/y4/mult4
y0/y4/mult4
Reg
Reg
x2
405(3)
x5
Cn
y0/y4/mult3
y0/y4/mult3
Reg
Reg
x3
405(4)
x4

FIG. 6

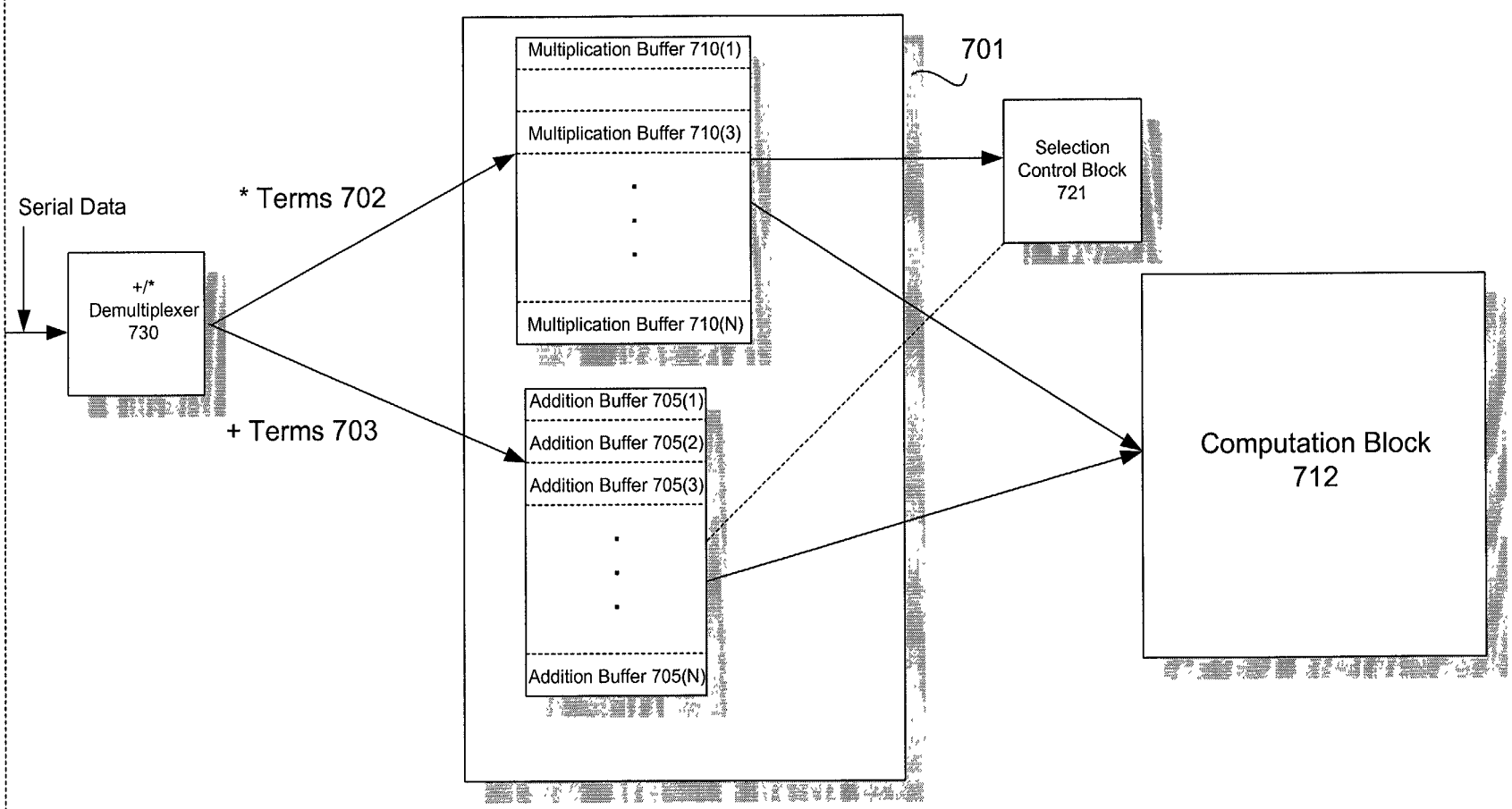

Serial Data
+/*
Demultiplexer
730
* Terms 702
+ Terms 703
Multiplication Buffer 710(1)
Multiplication Buffer 710(3)
Multiplication Buffer 710(N)
Addition Buffer 705(1)
Addition Buffer 705(2)
Addition Buffer 705(3)
Addition Buffer 705(N)
701
Selection
Control Block
721
Computation Block
712

FIG. 7

									x
		0	*1*	*2*	*3*	*4*	*5*	*6*	*7*
	0	0	1	5	6	14	15	27	28
	1	2	4	7	13	16	26	29	42
	2	3	8	12	17	25	30	41	43
	3	9	11	18	24	31	40	44	53
	4	10	19	23	32	39	45	52	54
	5	20	22	33	38	46	51	55	60
	6	21	34	37	47	50	56	59	61
y	*7*	35	36	48	49	57	58	62	63

FIG. 8a

									x
		0	*1*	*2*	*3*	*4*	*5*	*6*	*7*
	0	0	4	6	20	22	36	38	52
	1	1	5	7	21	23	37	39	53
	2	2	8	19	24	34	40	50	54
	3	3	9	18	25	35	41	51	55
	4	10	17	26	30	42	46	56	60
	5	11	16	27	31	43	47	57	61
	6	12	15	28	32	44	48	58	62
y	*7*	13	14	29	33	45	49	59	63

FIG. 8b

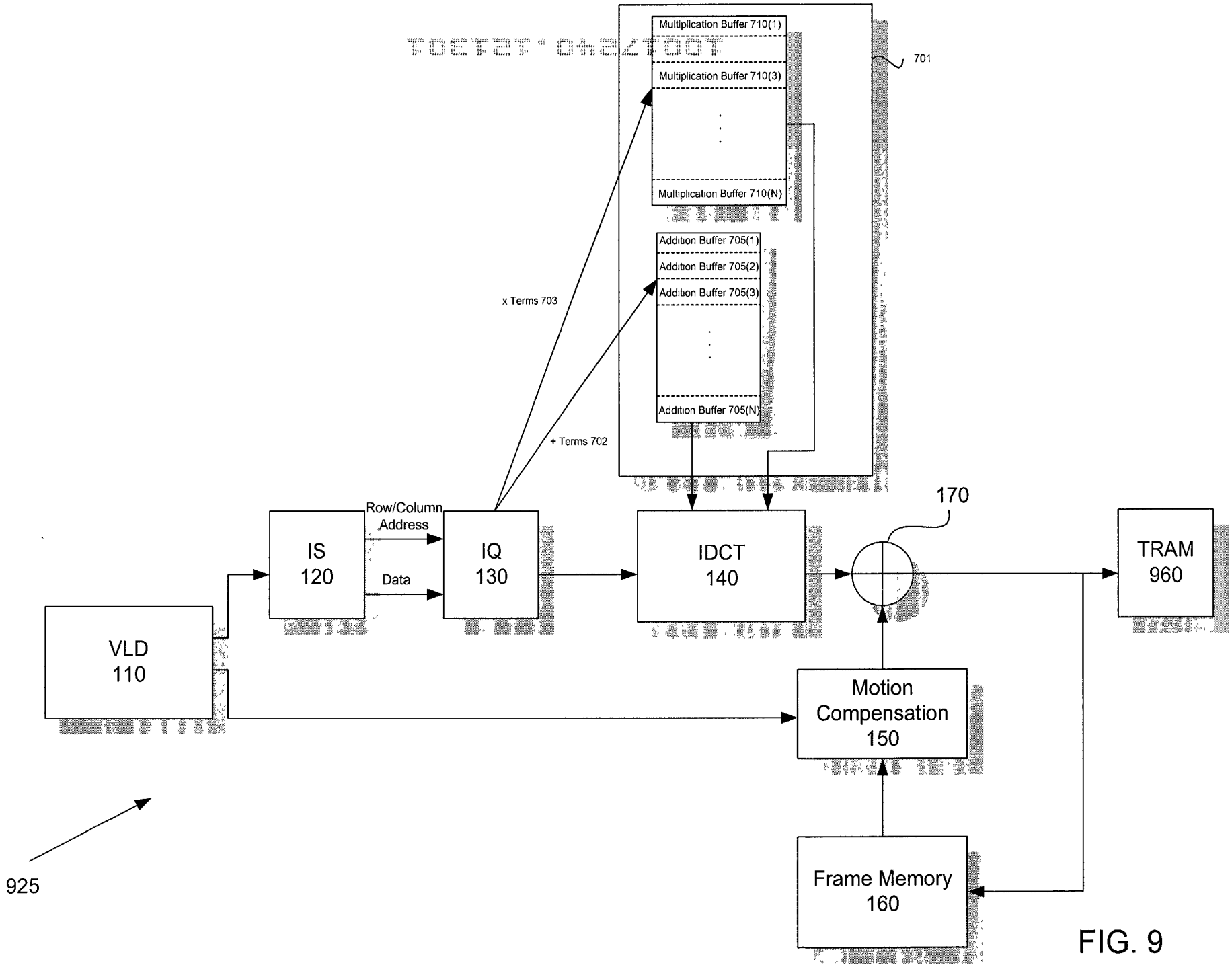

Multiplication Buffer 710(1)
Multiplication Buffer 710(3)
Multiplication Buffer 710(N)
701
Addition Buffer 705(1)
Addition Buffer 705(2)
Addition Buffer 705(3)
Addition Buffer 705(N)
x Terms 703
+ Terms 702
Row/Column Address
Data
IS 120
IQ 130
IDCT 140
170
TRAM 960
VLD 110
Motion Compensation 150
Frame Memory 160
925

FIG. 9

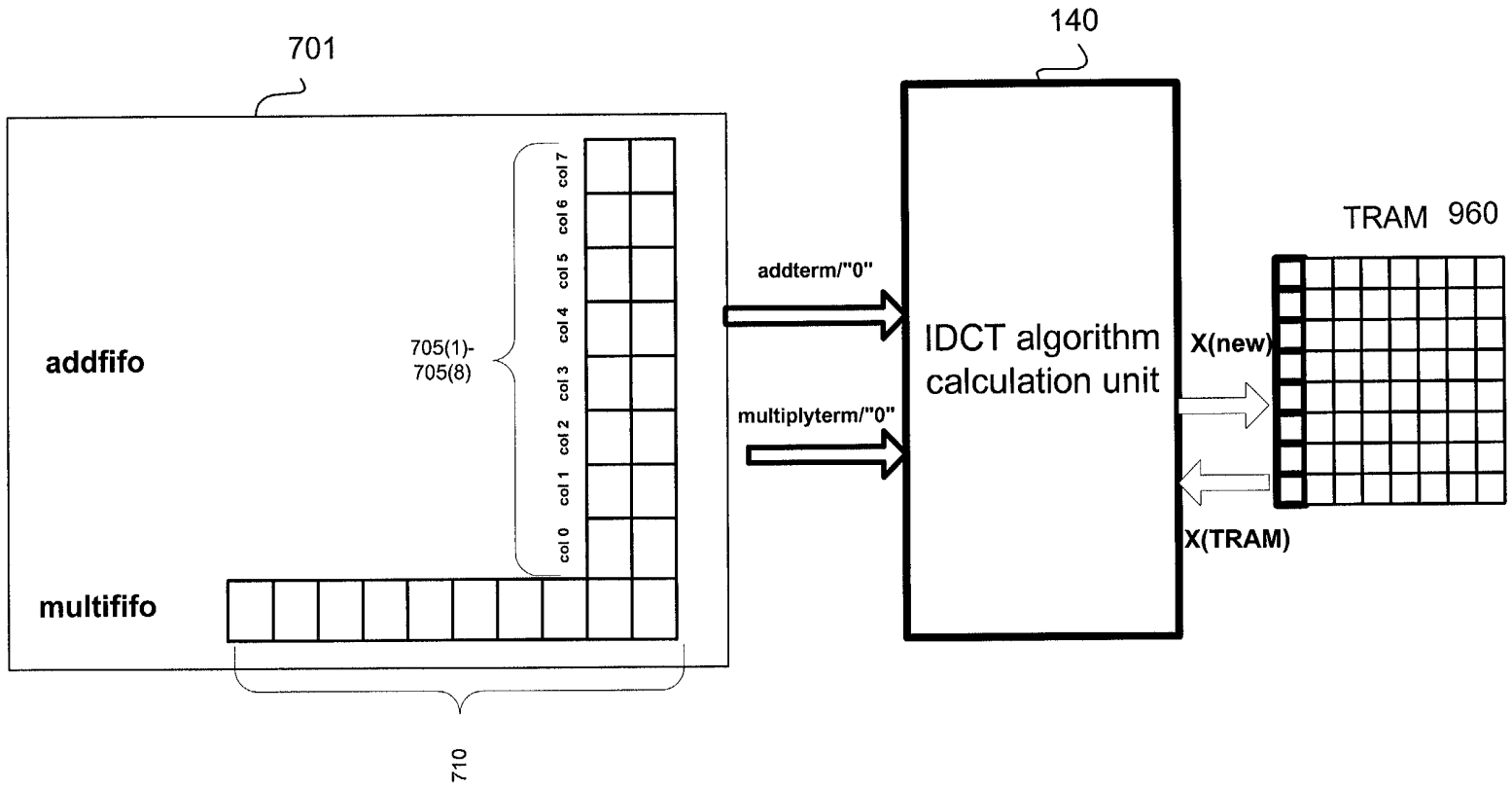


FIG. 10

									x
		0	1	2	3	4	5	6	7
	0	**0**	1	5	6	14	15	**27**	**28**
	1	2	4	7	13	16	26	**29**	42
	2	**3**	8	12	17	25	30	41	43
	3	9	11	18	24	31	40	44	53
	4	**10**	19	23	32	39	45	52	54
	5	20	22	33	38	46	51	55	60
	6	21	34	37	47	50	56	59	61
y	7	**35**	36	48	49	57	58	**62**	**63**

FIG. 11

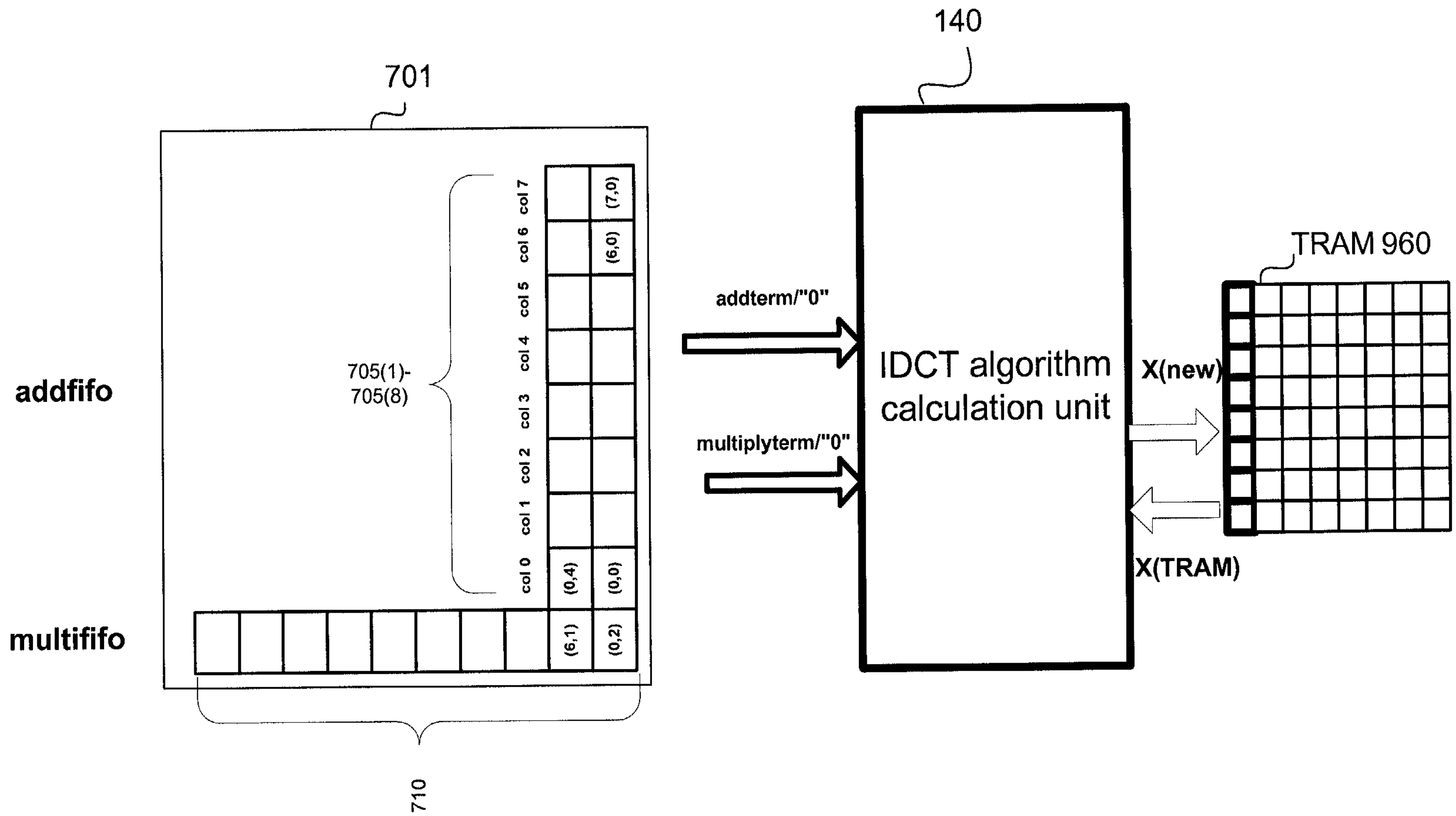
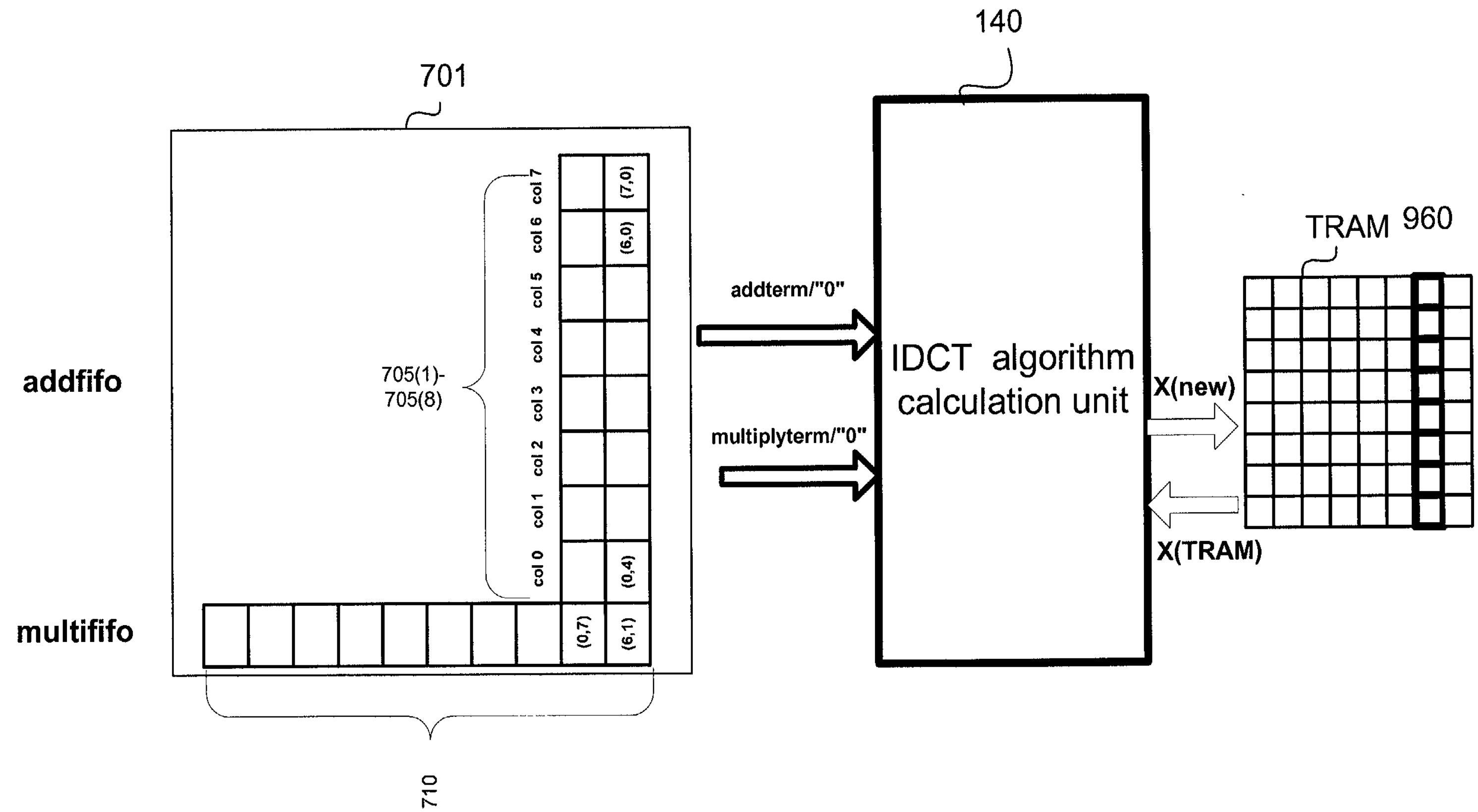

701
addfifo
multififo
705(1)-
705(8)
col 0
col 1
col 2
col 3
col 4
col 5
col 6
col 7
(0,4)
(0,0)
(6,0)
(7,0)
(6,1)
(0,2)
710
addterm/"0"
multiplyterm/"0"
140
IDCT algorithm
calculation unit
X(new)
X(TRAM)
TRAM 960

FIG. 12a



701
addfifo
multififo
705(1)-
705(8)
col 0
col 1
col 2
col 3
col 4
col 5
col 6
col 7
(7,0)
(6,0)
(0,4)
(0,7)
(6,1)
710
addterm/"0"
multiplyterm/"0"
140
IDCT algorithm calculation unit
X(new)
X(TRAM)
TRAM 960

FIG. 12b

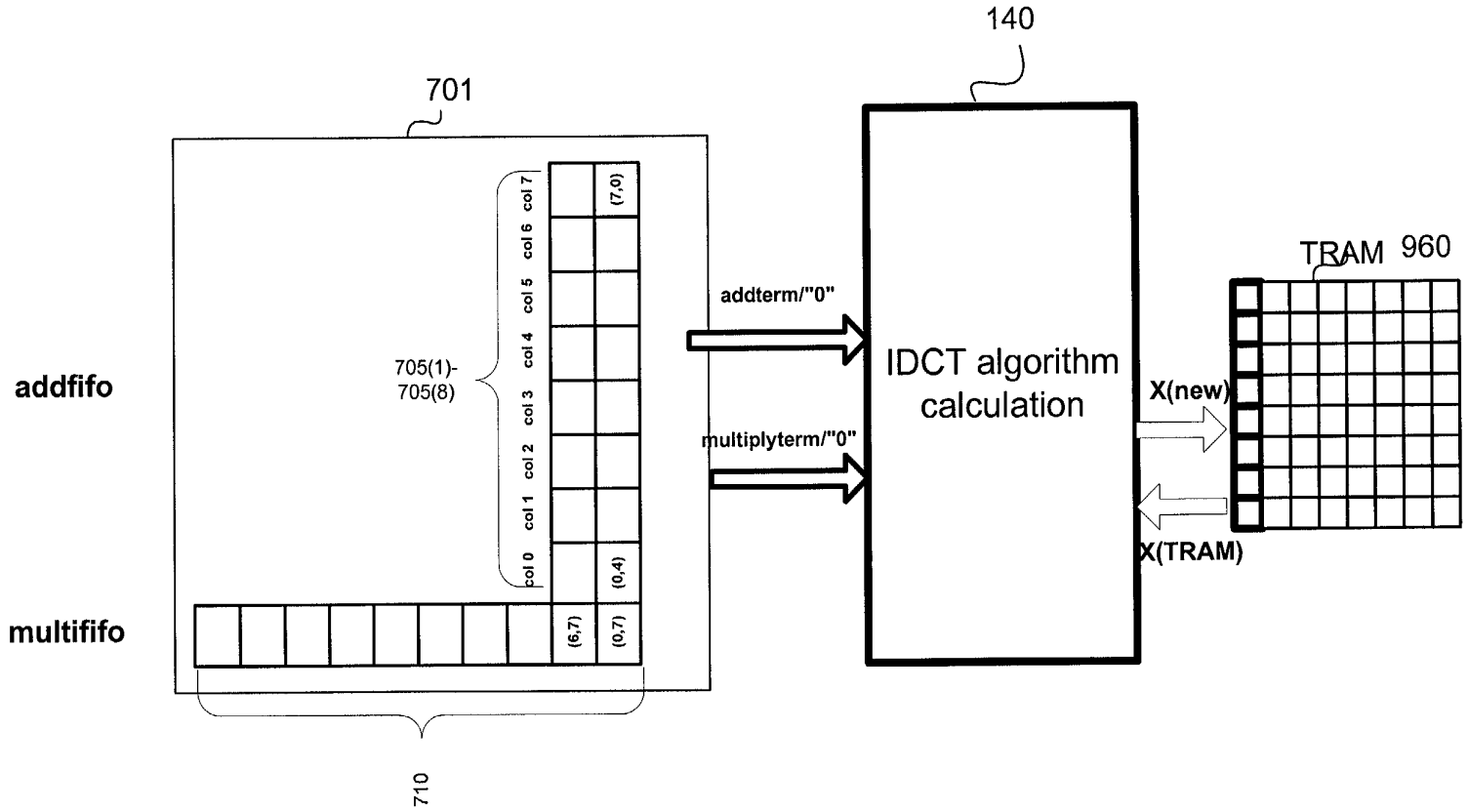

140
701
addfifo
multififo
705(1)-
705(8)
col 7
col 6
col 5
col 4
col 3
col 2
col 1
col 0
(7,0)
(0,4)
(6,7)
(0,7)
710
addterm/"0"
multiplyterm/"0"
IDCT algorithm
calculation
X(new)
X(TRAM)
TRAM 960

FIG. 12c

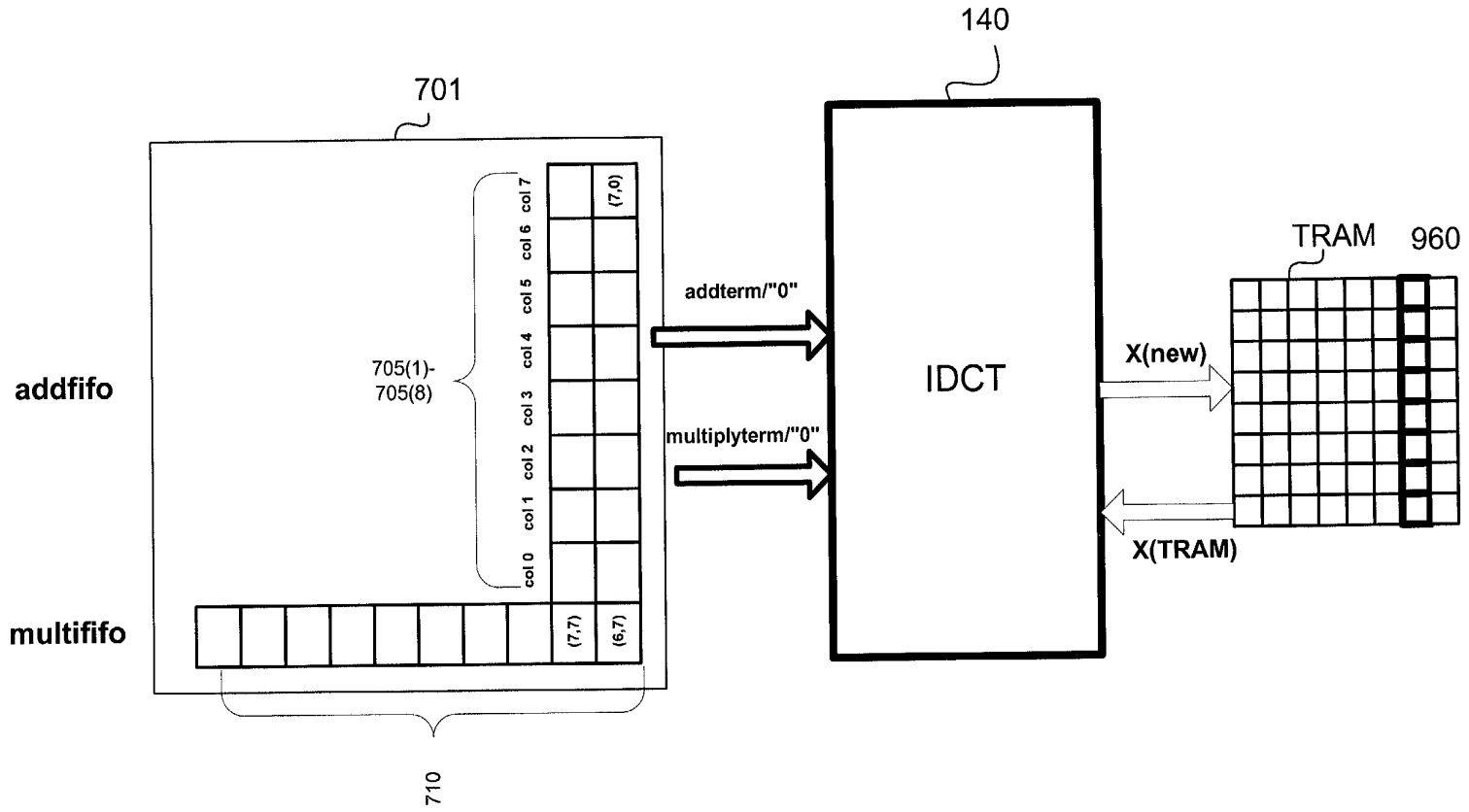


FIG. 12d

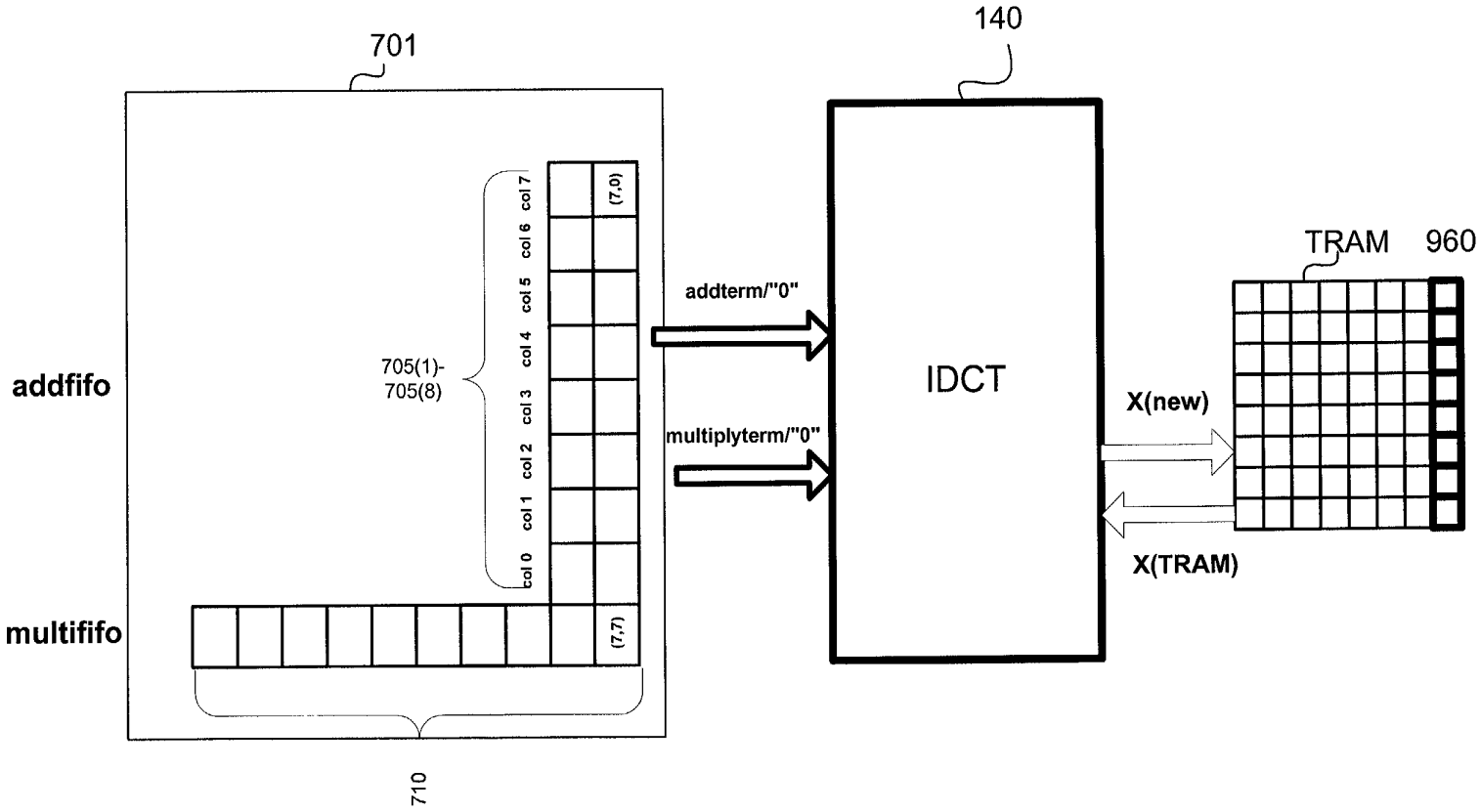

701
140
addfifo
multififo
705(1)-
705(8)
col 0
col 1
col 2
col 3
col 4
col 5
col 6
col 7
(7,0)
(7,7)
addterm/"0"
multiplyterm/"0"
IDCT
X(new)
X(TRAM)
TRAM
960
710

FIG. 12e

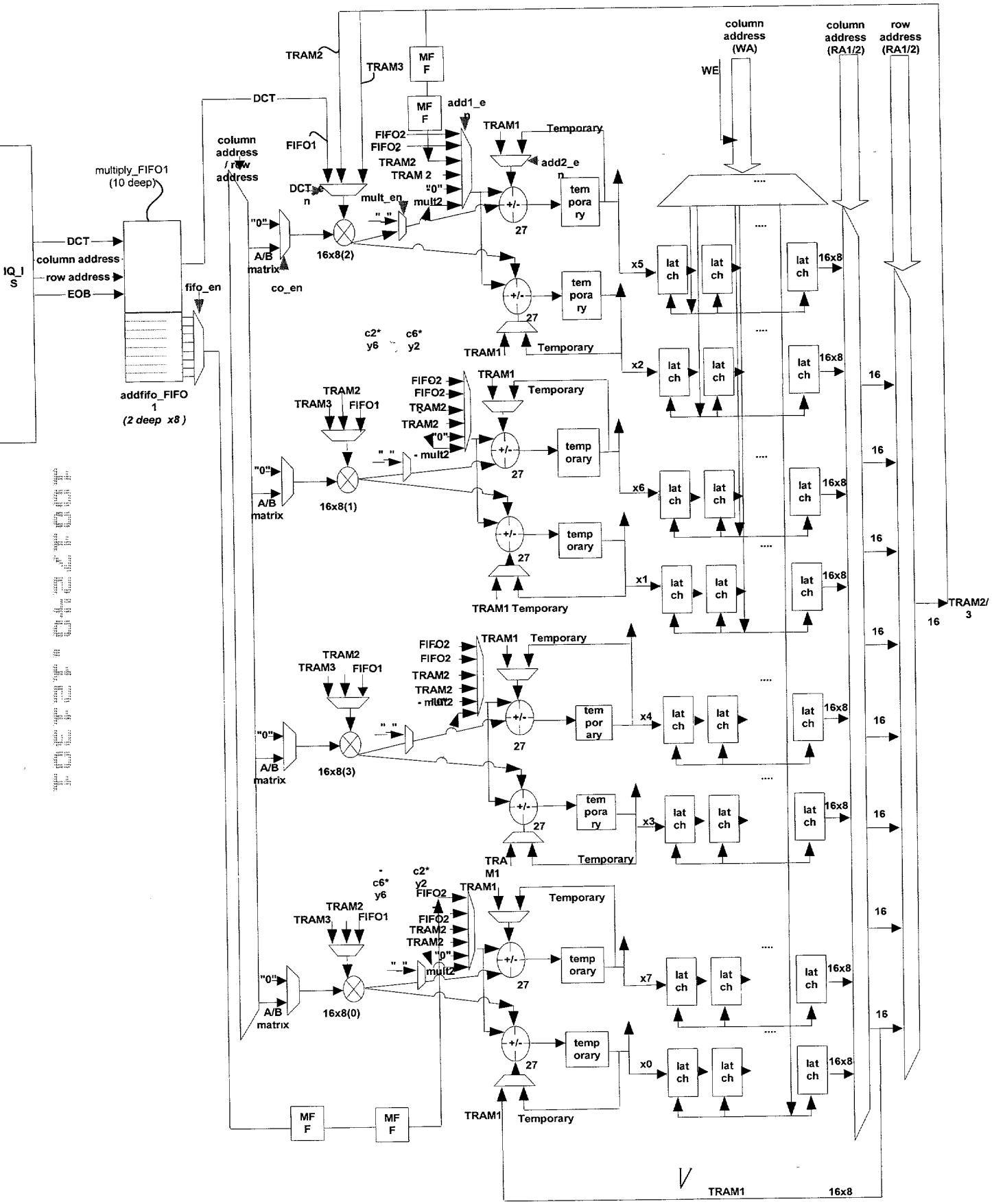

column address (WA)
column address (RA1/2)
row address (RA1/2)
WE
TRAM2
TRAM3
MF F
DCT
add1_e n
add2_e n
FIFO1
FIFO2
TRAM1
Temporary
TRAM 2
column address / row address
multiply_FIFO1 (10 deep)
DCT
column address
row address
EOB
fifo_en
addfifo_FIFO 1
(2 deep x8)
DCT_e n
mult_en
mult2
"0"
" "
A/B matrix
co_en
16x8(2)
16x8(1)
16x8(3)
16x8(0)
tem pora ry
temp orary
tem por ary
+/-
27
c2* y6
c6* y2
x5
x2
x6
x1
x4
x3
x7
x0
lat ch
16x8
16
TRAM2/ 3
TRAM1 Temporary
MF F
V
TRAM1
16x8

FIG. 13